# Improving full-wafer on-product overlay using computationally designed process-robust and device-like metrology targets.

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## ABSTRACT

In order to handle the upcoming 1x DRAM overlay and yield requirements, metrology needs to evolve to more accurately represent product device patterns while being robust to process effects. One way to address this is to optimize the metrology target design. A viable solution needs to address multiple challenges. The target needs to be resistant to process damage. A single target needs to measure overlay between two or more layers. Targets need to meet design rule and depth of focus requirements under extreme illumination conditions. These must be achieved while maintaining good precision and throughput with an ultra-small target. In this publication, a holistic approach is used to address these challenges, using computationally optimized metrology targets with an advanced overlay control loop.

**Keywords:** Holistic, target design, On Product Overlay, multi-layer, DBO, D4C, metrology, precision, throughput, accuracy, process robustness, device matching, DRAM, tilted structures, extreme illumination.

## 1. INTRODUCTION

Overlay metrology target design has been identified in recent years as a potential way to improve overlay performance through the optimization of target performance for a given process stack[1]. To get the best possible metrology input into the APC feedback loop, the focus in target design has turned to overlay accuracy. In this case, accuracy refers to how similar a metrology target behaves with respect to the actual critical device pattern overlay. Historically, target design had been limited to empirical trial and error methods where several targets were added to successive reticle tape outs, measuring a specific set of metrology-related performance indicators such as precision, overlay error residual or more recently, the CD-SEM based measurement of device like overlay structures at the post etch step – considered to be a reference for accuracy. Advances in process technology such as double patterning or the extreme illumination needed for resolution enhancement techniques (RET) have resulted in a bigger challenge to design working metrology targets with sufficient detectability performance, even before concentrating on the bigger pay off of more accurate metrology. These process requirements in turn increased the number of experiments and tape outs required to find reliable targets. In order to reduce the development time, the simulation of the optical behavior of metrology target designs in the process stack has therefore become more common. Primarily this had been used more to ensure that at least some of the experimental targets would work at all. The concept of making metrology targets optimized to actually improve overlay performance and ultimately device yield has only gained prominence in recent years.

Big challenges exist in both lithography and non-lithography process steps so that finding targets that will be printable, having satisfactory process window, precision, throughput and overlay residual error or accuracy requirements. Trying to find a metrology target that simultaneously meets all of these requirements is no longer feasible within the time allotted when using only empirical methods. This work shows how computational methods help solve several of the challenges involved.

Metrology, Inspection, and Process Control for Microlithography XXIX, edited by Jason P. Cain, Martha I. Sanchez, Proc. of SPIE Vol. 9424, 942414 · © 2015 SPIE
CCC code: 0277-786X/15/$18 · doi: 10.1117/12.2085645

## 2. BACKGROUND

Designing metrology targets that mimic device behavior by design is becoming a key component of overlay process control. The extreme illumination methods needed for DRAM technologies make it harder to control the aberration induced overlay delta between metrology target and device patterns. This mismatch can be minimized through the right choice of targets and measurement recipe to support achieving the best possible on-product-overlay performance and device yield.

In contrast to a traditional 'trial and error' approach, ASML's Design for Control (D4C) simulation software provides a systematic computational methodology for small diffraction based overlay (μDBO) target design with dimensions of 16μm by 16μm or smaller. It can optimize targets for all required metrology metrics. In this work, we applied a holistic methodology of target design using 4 building blocks – the combined optimization of Printability, Detectability, Robustness and Device Matching.

To speed up the process of finding optimal DBO targets to place in both development and HVM process reticles, the D4C software was used. Through simulation of the nominal process properties as well as expected variations, we were able to save considerable time in finding the optimal balanced target. We then applied these optimized targets to high volume manufacturing on a 20nm DRAM production environment, using ASML's YieldStar metrology system with an advanced overlay feedback control loop.

## 3. HOLISTIC TARGET OPTIMIZATION

Holistic can be defined as "relating to or concerned with complete systems rather than with individual parts". Holistic solutions have been applied with increasing success to lithographic and other fab processes in recent years. Now that the challenge of designing good metrology targets for cutting edge process nodes is becoming unmanageable by experimental methods, it's a logical step to try to solve this problem holistically through computational means.

To enable this, competencies in the areas of metrology, lithography and process integration need to be leveraged to place targets that are effectively "process aware". First we need to consider how the target will be patterned in the lithography and etch steps. This includes the challenge of the tilted pattern structures of a DRAM device, along with the extreme illumination shapes needed to pattern them. Next we need to optimize the targets detectability by simulating the optical behavior of a diffraction grating in a process stack when measured by a YieldStar overlay metrology system. Then we need to look at the robustness of targets if non-overlay-related variations were to occur either within wafer or from wafer-to-wafer. Finally we need to work on the key goal of making targets that are less sensitive to the asymmetry in the target grating caused by non-lithography processing steps like etch or chemical mechanical polishing.

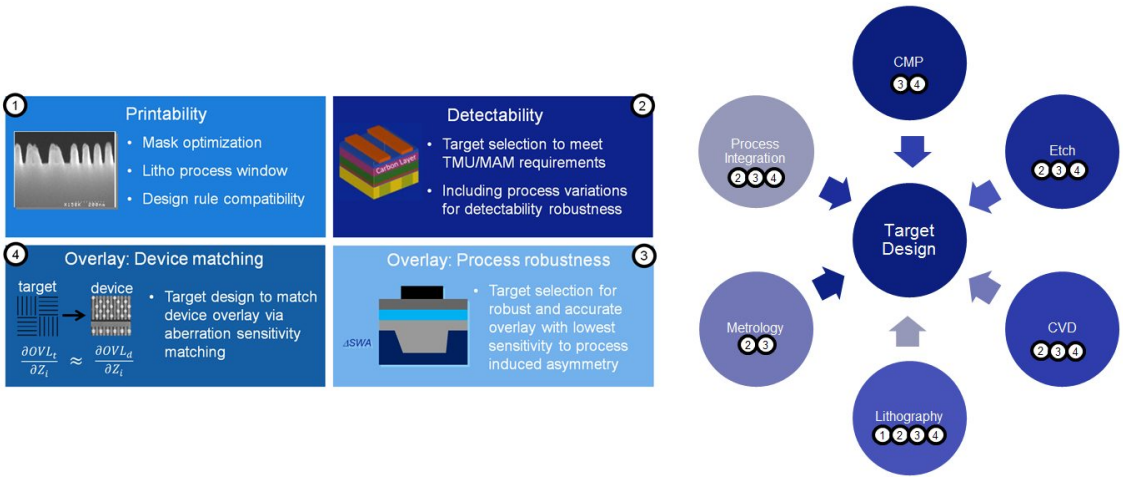


Figure 1. Holistic Target Optimization considers multiple process factors influencing overlay metrology target performance

A step by step process has been adopted to ensure minimal iterations in the simulation process while optimizing each of the 4 key components. Device rules are set and a selection of compatible targets undergoes the co-optimization process to find a target which has the best balance of all of the performance metrics.

## 4. PRINTABILITY

Traditionally overlay metrology marks are placed on the reticle as is, due to the relatively large dimensions and ease of imaging. However this situation changes with the use of extreme dipole illuminations. Figure 2. shows the various target pattern types, including non-segmented targets and segmented targets with parallel or tilted arrays, which can have extremely low depth of focus that do not survive small focus variations that are naturally present across the wafer. To overcome this requires sophisticated model-based OPC and RET techniques such as sub-resolution assist features to boost the depth of focus.

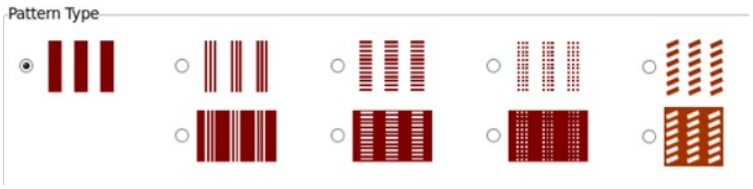


Figure 2. Examples of the target pattern segmentation types available for a µDBO grating

Several RET techniques were used in an attempt to make sure that the best performing targets from a detectability point of view would also be printable on a wafer and robust to other process steps such as CMP. As part of the simulation study, several types of parallel or tilted grating segmentation types were tried either at or close to critical product pitches based on the illumination shape. Non-segmented targets were also simulated but expected to have problems with other processes which could lead to defects. Each time, the DOF of a potential candidate target was verified.

Figure 3. shows the focus window for two different types of target grating pattern. The first is a structure without OPC. While this grating meets the criteria for detectability performance before any OPC is applied, it cannot meet the required focus window for this process and is therefore at risk of causing some defects which could impact yield. The second grating shows the focus window after OPC is applied. This increases the depth of focus to approximately 120nm making it usable without risk to production.

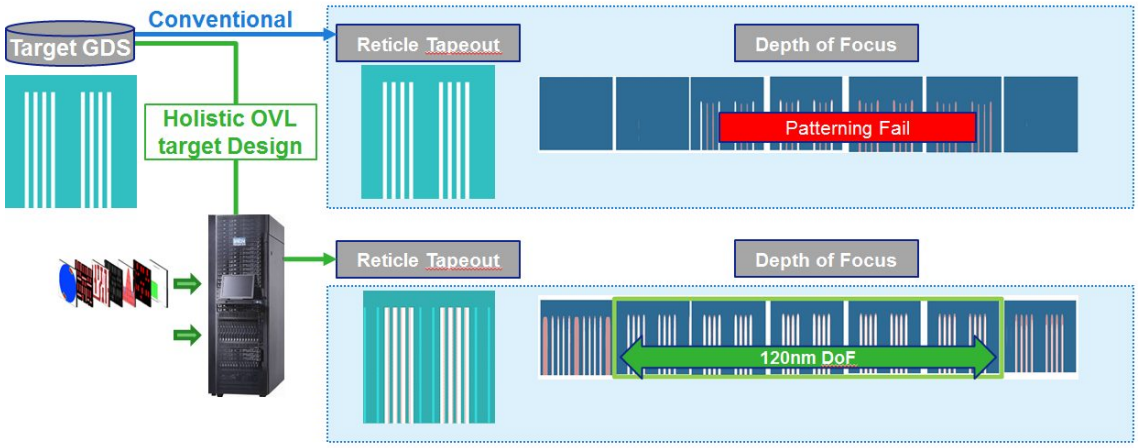


Figure 3. The structure segmentation needed for accurate targets require sophisticated OPC and signal simulation techniques. More than 120nm in depth of focus can be achieved with OPC on a target that previously could not even pattern.

## 5. DETECTABILITY

At each new technology node, the shrinking device size and more challenging overlay performance specs require higher order corrections and therefore spatially denser sampling. This can only be done without undue impact on die size if the targets are sufficiently small. Measuring more targets also means less time to measure. Therefore it is of great importance that we can measure small targets very quickly. This requires effort to always ensure better and better target detectability performance. At the same time, the requirements of cutting edge process technologies such as multiple patterning and increased thicker opaque materials in the process stack combine to result in a lower duty cycle in the target grating pattern which causes the signal to noise performance and hence precision of the target to get incrementally worse. As a result, many targets that used to work well will no longer meet the requirements. Using simulation we are able to quickly sift through thousands of target dimensions to look for ones that give the performance that meet detectability requirements.

The simulation and analysis methodology allows us to identify a target that will be able to reach a threshold of total measurement uncertainty (TMU) and move-acquire-measure (MAM) time with 'sufficiently good performance' so that we can focus on the more critical performance indicators which actually affect overlay performance such as Process Robustness (accuracy) or Device Matching.

Another challenge that has been added in recent years comes from the introduction of combined or multi-layer targets, where it has sometimes been necessary to have a single target which measures between more than the traditional two layers. The consequences of this is a requirement to select gratings for the overlay measured so that, if possible, all layers can be measured with a single metrology tool recipe condition. The benefits of this will come from not having to run multiple recipes for measurement and hence avoiding an increase in measurement time.

In Figure 4 an example of the analysis of simulation results of the key detectability metrics is shown. By simulating thousands of combinations of pitch, CD, segmentation type, it is possible to find an optimal target. This case shows the simulation used to redesign a target after the process stack had changed. It was possible to identify a target which would meet all necessary target design criteria with excellent detectability performance. The simulations were also later confirmed by measurement on the metrology tool. The next step in the design phase is to ensure these targets are robust for potential process variations.

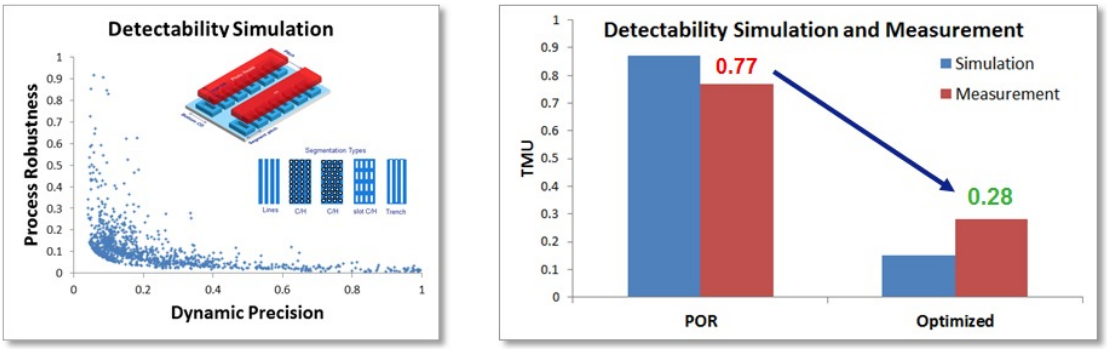


Figure 4. Several combinations of target dimensions are simulated and an optimal target is found which balances detectability metrics ensuring optimal precision performance. The benefit of target optimization has been confirmed in both simulation of a precision metric and measured TMU.

## 6. DETECTABILITY ROBUSTNESS

To design stable targets that perform well and have no risk of failure during High Volume Manufacturing, the simulation technique needs to also consider the potential process variations that could occur to parameters such as material thickness. An ideal target should be robust against the temporal, spatial, and process tool-population differences that are immaterial to actual critical-pattern-on-product overlay. Targets need to be designed to meet their performance metrics across the full space of all expected combined process variations. In contrast to the experimental method of exploring target performance, this challenge can be handled with relative ease using simulation, saving the need to design multiple test wafers with all expected variation combinations. Typical expected amounts or process variation can be added to the simulation perturbations to predict the impact to detectability performance. In Figure 5, the methodology is shown where the performance indicators are predicted and the variation caused by expected process variation is shown by the error bars. Then the targets highlighted in green are selected because they meet threshold performance metrics even when the process varies or drifts.

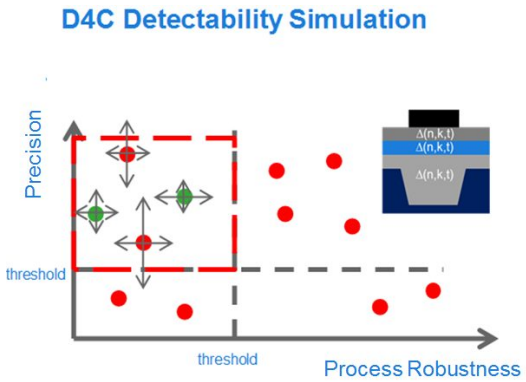


Figure 5. The detectability robustness is found by simulating target performance for a spread of expected process variations

In addition to process variation, the target must also maintain a physical robustness to mechanical or chemical damage or interference from surrounding or underlying structures. In order to do this, typically target protections techniques such as shielding or adding dummy structures are applied based on a combination of the given layers design rules, experience and experimentation. Once again, simulation makes it possible to verify the performance of targets with this protection up front, without the need for time consuming and expensive empirical testing.

## 7. PROCESS ROBUSTNESS – ACCURACY

Optimizing a target for Process Robustness or accuracy means minimizing the sensitivity to target grating asymmetries which are induced by process steps such as etch or CMP. These asymmetries affect the perceived overlay measured by the metrology tool and can occur both systematically and randomly. The goal in target design is to reduce the sensitivity to the asymmetries which are expected to occur for a given stack.

The measured performance of several targets is shown for a given 20nm DRAM layer (Figure 6). In this case, several μDBO target/recipe combinations of varying asymmetry sensitivities were measured. Measured Accuracy refers to the 3 sigma of the point-to-point delta between Yieldstar Overlay and the CD-SEM measurement of overlay on device like structures. The Simulated Accuracy refers to predicted overlay to a given combination of asymmetries on the metrology target grating. There is little correlation, however, between these and the old metric for metrology target performance (TMU).

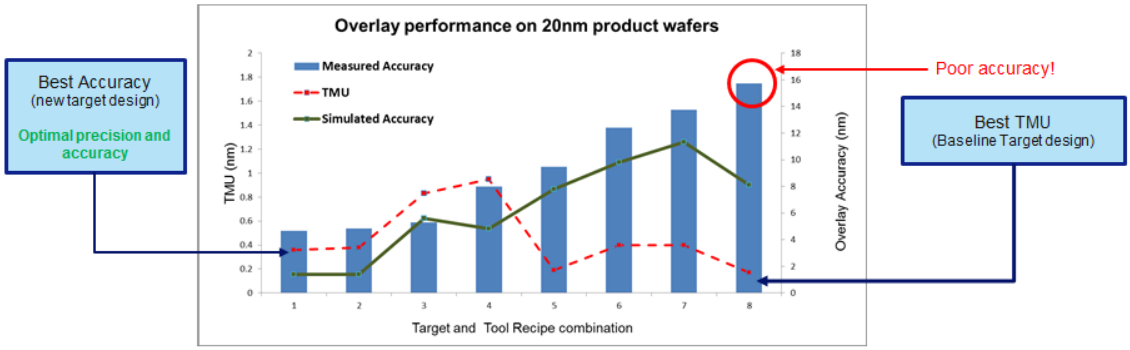


Figure 6. Overlay targets are selected based on confirmation of device cell matching (accuracy). Here the TMU is confirmed to have poor correlation to this key accuracy metric. Simulation can predict which target has lowest sensitivity to asymmetries.

It has also been observed experimentally using scatterometry based CD reconstruction of the Side Wall Angle (SWA) of DBO target gratings, that when the grating asymmetry varies across a wafer, the overlay measured will also vary depending on the target sensitivity (Figure 7). Therefore it's possible to design through simulation and select a target which has the optimal (minimal) sensitivity to asymmetry. D4C could predict a target which had very little overlay error across the wafer even when the asymmetry was observed to have changed.

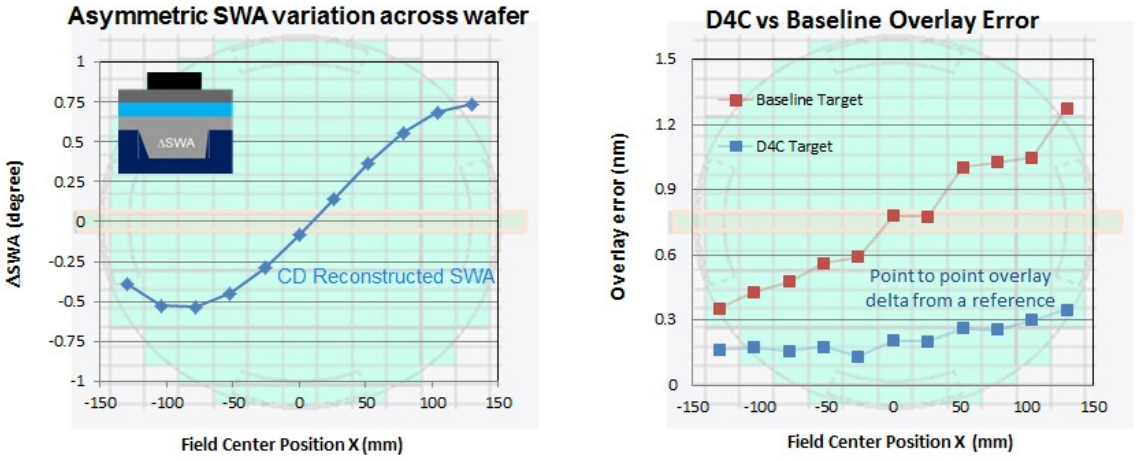


Figure 7. Asymmetric SWA across a wafer can impact the measured overlay. Targets with reduced sensitivity to asymmetry can be therefore selected through simulation. This will result in improved accuracy.

## 8. DEVICE MATCHING

Three specific points need to be considered when trying to ensure that a metrology target is matched to the device as close as possible. Firstly, it's required that the shape and dimensions of the target are constructed from patterns that are process compatible. For a start, this will ensure that the process artifacts which change the device behavior will change the target in a similar way. This could also apply to the mechanical artifacts on the target profile added during the CMP process steps. Secondly, we should ensure the optical artifacts from the lithography pattern steps due to aberrations resulting from lens heating effects are minimized. And thirdly, it's necessary to choose a target for which the Yieldstar metrology tool will have the least sensitivity to the above mentioned asymmetries which may occur due to lens aberrations. Figure 8 shows the sensitivity of the top and bottom targets of a given layer. The sensitivity of the bottom target grating in the x direction was observed due in large part to Z10, Z11 and Z26 Zernikes.

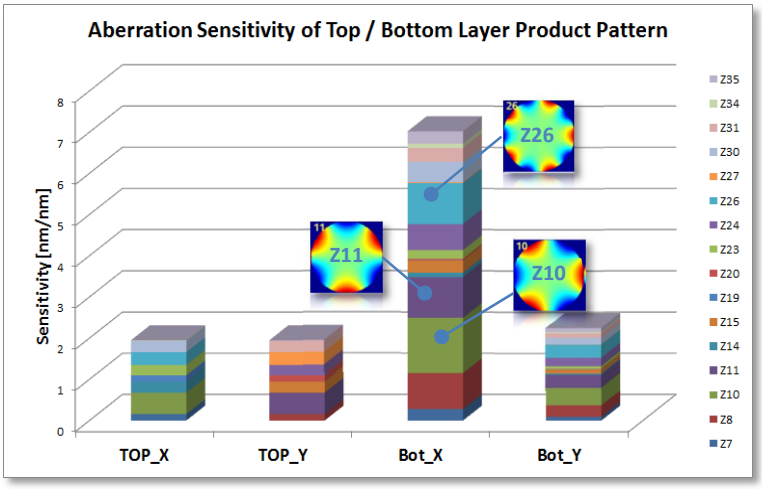


Figure 8. Aberration Sensitivity refers to the sensitivity of the Yieldstar sensor to asymmetry caused by patterning. A high sensitivity to specific Zernikes was observed.

In a DRAM process, this means it can often be optimal to use targets which are segmented so that they behave similar to the device. In some cases, where patterning a target grating with tilted structures is not possible without defect or process window limitation concerns, the next closest printable pattern will be used such that the asymmetry sensitivity is minimized. Considering the extreme illumination shapes used for active area, this step may often require smart RET techniques on the target. Computational design eases this process and a method of simulating printability, applying OPC and then checking the metrology performance metrics for the sensitivity to asymmetries of printable targets saves considerable experimental effort.

There are multiple benefits to this design process. The need to confirm that metrology correlates well enough to device like structures by CDSEM, e-test or ultimately yield can be reduced, and earlier identification of mismatch allows issues to be fixed up front. The need to apply corrections to these offsets could be done in advance by a feed-forward method or, more preferably, the need to correct can be almost entirely removed.

In order to design targets that match device overlay, we must be able to rely on model prediction of the overly errors between target and device. In the example below (Figure 9a), we show the simulated through slit fingerprint of the overlay error caused by the aberration sensitivity of a µDBO target. In the same plot, we then see the measured overlay delta between the actual printed µDBO target and the device like CDSEM target. This shows that simulations can accurately predict the overlay target delta to cell matching. AS a result it has become possible to metrology targets whose aberration sensitivity matches closely to the device cell using OPC (Figure 9b).

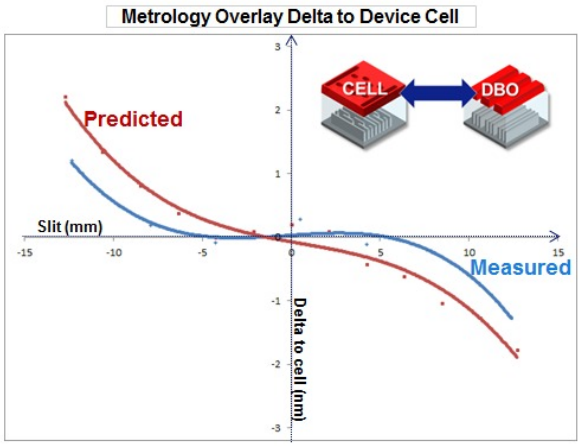


Figure 9a. Predictions of aberration sensitivity match well to actual on-wafer measurements of cell matching

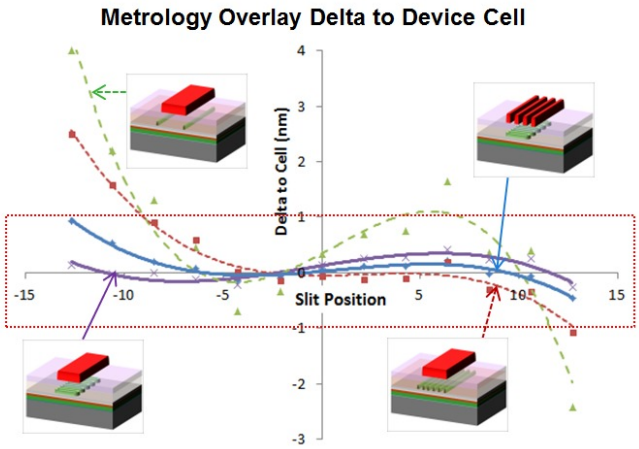


Figure 9b. The ability to predict aberration sensitivity then allows the identification of optimum pitch, cd and segmentation

## 9. HOLISTIC OVERLAY

The primary success criterion of a metrology mark optimization activity is an increased die yield, as predicted by reduced measured overlay between critical cell features. The ability of a metrology mark to enable optimum feedback corrections is dependent upon precision, accuracy, and robustness against process deformation. In addition, a carefully implemented overlay control strategy is needed, with model and sampling tuned to minimize any remaining metrology noise. Figure 10 shows the Mean of 3sigma wafer overlay, for a production split of 20 lots, in 20nm DRAM production. In virtually all cases the split with the optimized mark reduces both measured (Raw) overlay, and the residual (Res) overlay which cannot be described by the automatic process control model (APC).

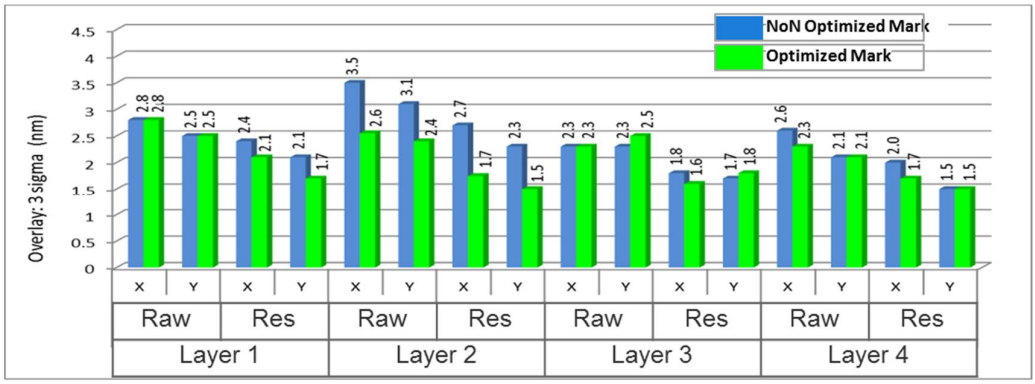


Figure 10. Mean performance improvement with optimized targets over previous targets in both raw and residual overlay

The correlation of overlay metrology technologies, such as image based or diffraction based overlay, to critical device overlay tends to decrease towards the wafer edge. By carefully matching overlay data, to a series of CD-SEM cell measurements, a detailed map of the inaccuracy can be derived. Again, the cell matching data can be separated into the systematic difference which is APC correctable, and the residual to this model, which will disturb feedback control as a source of noise.

Figure 11. shows that a large cell matching improvement is obtained with the optimal target choice, and that the residual overlay shows a significant reduction due to the computational mark design method.

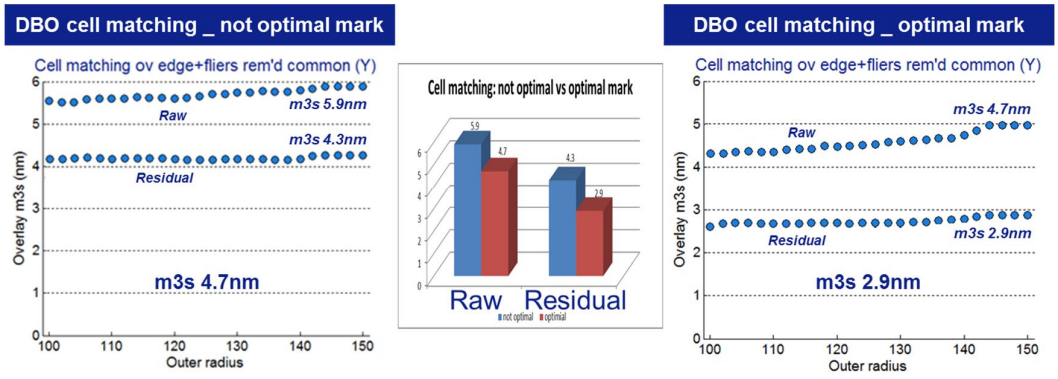


Figure 11. The gain in full wafer product cell matching accuracy with an optimized target design

When viewed on the wafer level (Figure 12), the detailed correspondence of the measured fingerprint to real cell behavior becomes apparent. The remaining inaccuracy can in part be explained as a combination of the precision of both DBO and SEM metrology tools.

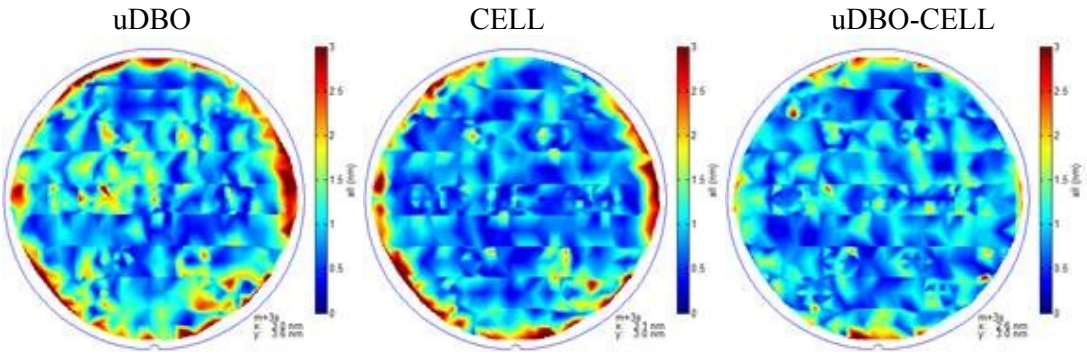


Figure 12. Full radius wafer matching to product cell overlay shows good cell matching with an optimized uDBO target

With a holistic metrology and control strategy, which begins with computational simulation of realistic process stacks, it becomes possible to design and simulate directly for performance in accuracy terms, as well as the traditional precision. This enables advanced predictions of Yield performance, with die-aware, edge optimized correction models and sampling. In the case of 20nm DRAM production, a 2.5% yield improvement was predicted after an optimized target and sampling optimization we adopted (Figure 13), and with implementation underway, final verification is expected on an upcoming product revision.

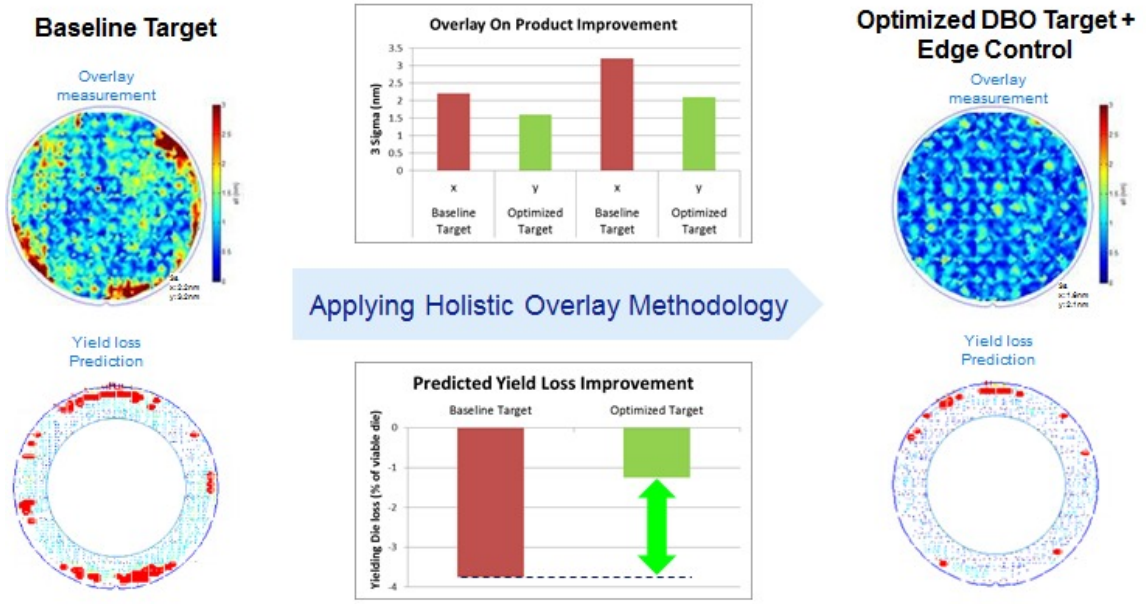


Figure 13. Overlay performance and wafer edge yield loss prediction before and after optimization of the target and sampling scheme. Using an optimized target and sampling plan shows clear potential benefits for overlay and yield performance.

## CONCLUSION

Using a holistic method of target design, μDBO in combination with an advanced feedback system has shown performance benefits which can be applied to High Volume Manufacturing on a 20nm and DRAM process. The biggest single benefit is in the ability to design printable targets which mimic the device cell pattern sensitivity to process dependent asymmetries. When combined with optimized feedback and sampling, a holistic feedback loop using metrology measurement more closely represents the device behavior and can have a positive impact on overlay and yield performance.

For a DRAM process this is a very challenging problem which could only be solved through a combination of process knowledge and simulation techniques. Metrology targets can be designed for their robustness to process variations, ensuring the detectability performance will always meet a required threshold irrespective of variations in the process in a high volume scenario.

Overall, it has become possible to reach better and more consistent overlay performance sooner by means of a holistic target design and feedback system. The step by step approach described in this paper allows the best target to be found without the need for multiple iterations of reticle tape outs and empirical validation of multiple targets. Optimizing a key set of target performance KPIs leads to a target which performs better overall when taking into account all of the critical metrics such as TMU, MAM, Overlay Residual and Accuracy.

The contribution of robust, accurate mark design to device-performance critical overlay, in the typically low-yielding wafer edge area (beyond 140mm of wafer radius) has been demonstrated, including the value of the computational approach. With an in-depth understanding of the role of process induced variation, and metrology induced variation, an optimum correction strategy has been developed, and implemented for 20nm DRAM production, where final yield verification is underway.

## ACKNOWLEDGEMENTS

The authors would like to thank the ASML Korea Field Applications team for measurement and analysis support and Neal Callan, Bob Socha and Ronald Goossens for their support in writing this paper.

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